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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/609,567	06/30/2000	Robert D. Bateman	042390.P9220	2886

7590 06/03/2004  
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EXAMINER

THAI, TUAN V

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 06/03/2004

17

Please find below and/or attached an Office communication concerning this application or proceeding.

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# Office Action Summary

Application No.

09/609,567

Applicant(s)

BATEMAN, ROBERT D.

Examiner

Tuan V. Thai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 29 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-8, 11-14, 17 and 19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 11, 13, 14, 17 and 19 is/are rejected.
- 7) ☒ Claim(s) 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 June 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_.

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**Part III DETAILED ACTION**

***Response to Amendment***

1. This office action is in response to Applicant's communication filed March 29, 2004. This amendment has been entered and carefully considered. Claims 1-8, 11-14, 17 and 19 remain pending in the application. Claims 9-10, 15-16, 19 and 20-22 have been canceled.

2. Applicant's arguments with respect to claims 1-29 have been considered but are deemed to be moot in view of the new grounds of rejection.

***Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 11, 13-14, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (USPN:

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5,956,744); hereinafter Robertson.

As per claim 1; Robertson teaches the invention as claimed including a method for storing data in a cache comprising prioritizing locked way of the cache higher than a recently used way (e.g. see column 22, line 33 bridging column 23, line 10); specifically, starting at lines 34 et seq., Robertson clearly discloses it is beneficial to ensure the cache entries expected to be used most often would not be replaced ***even if they are the least recently used by employing the priority lock level PL[1:0]*** wherein the locked priority is the highest priority (even if it is not the least recently used entry/way; e.g. see lines 53-54). Robertson, with one exception, does not particularly disclose prioritizing an additional locked way higher than the locked way. First of all, it should be noted that, even though Robertson discloses "the locked priority is the highest priority" (column 22, lines 53-54), this 's merely in reference to a single level priority (column 22, lines 50 et seq.); Robertson, on the other hand, goes on and details multi-priority levels wherein Robertson states that particular encoding of priority level PL[1:0] is ***merely a convenient design choice. The priority level could include two levels or more than three levels*** (e.g. see column 22, lines 63 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current

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invention was made to readily recognize that different ways of the cache can be independently locked in different levels (column 23, lines 3 et seq.), and by assigning different priority levels to different lock ways or "prioritizing an additional locked way higher than the locked way", it would minimize errors in executing and processing data in different ways of the cache, which results to enhancing of system reliability, therefore being advantageous.

As per claim 2, storing data in the least recently used way (e.g. see column 6, lines 12 et seq.; column 22, lines 48-50);

As per claim 3, Robertson discloses prioritizing the locked way higher than a least recently used way and storing data in the least recently used way (e.g. see column 22, line 33 bridging column 23, line 10);

As per claim 4, locking at least one way/entry of the cache to provide the locked way (e.g. see column 22, lines 54 et seq.);

As per claims 5 and 8, the further limitation of reading/writing data from/to a way (entry) of the cache prior to prioritizing the locked way wherein the way being the recently used way is embedded in the system of Robertson since (a) Robertson, in fact, discloses the concept of prioritizing the locked way to be the highest priority level even though the way being the least recently used way (e.g. see arguments with

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respect to claim 1); in addition (b) data from cache is always being accessed (read/write) regardless of before or after the prioritizing operation in order to carry out the prioritizing/lock operation;

As per claims 6-7, Robertson discloses setting a bit in the parameter section 420, PL[1:0] bit, to indicate the prioritizing of the locked way, the way could be least-recently-used way (e.g. see column 21, lines 28-29; column 22, lines 63 et seq., figure 6); Robertson further discloses the priority level for each cache entry/way may be stored in a cache priority look-up table (register as being claimed) (e.g. see column 6, lines 19-20);

As per claim 11, setting the first and second bits of the register to indicate priority of the locked/additional-locked/LRU way is taught by Robert as setting a bit in the parameter section 420 for each cache entries, PL[1:0] bit, to indicate the prioritizing of the locked way (e.g. see column 21, lines 28-29; column 22, lines 63 et seq., figure 6);

As per claims 13 and 17, see arguments with respect to claim 1; in addition, Robertson discloses the invention as claimed including an apparatus comprises a cache (cache 305, figure 5) having multiple ways/entries including first and second ways (e.g. see column 22, line 20), locking a first way/entry of a cache (table 4 on column 22, when PL[1:0] status at [1:1]; also see line 54 et seq. on the same column); accessing a second/third

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way of the cache is taught as other cache entries of the six entries of cache 305 are accessed for data (cache 305 is full (e.g. see column 22, lines 20-26), prioritizing the first way of the cache higher than the second way of the cache is equivalent taught as locked way/entry having highest priority (e.g. see column 22, lines 53-54);

As per claim 14; Robertson discloses setting a bit in the parameter section 420, PL[1:0] bit, to indicate the prioritizing of the locked way, the way could be least-recently-used way (e.g. see column 21, lines 28-29; column 22, lines 63 et seq., figure 6); Robertson further discloses the priority level for each cache entry/way may be stored in a cache priority look-up table (register as being claimed) (e.g. see column 6, lines 19-20);

As per claim 19, Robertson further discloses the priority level for each cache entry/way may be stored in a cache priority look-up table (register as being claimed) (e.g. see column 6, lines 19-20).

#### **Allowable subject matter**

5. Claim 12 is objected to as being dependent upon a rejected based claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

#### **Conclusion**

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (703) 305-3842. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may



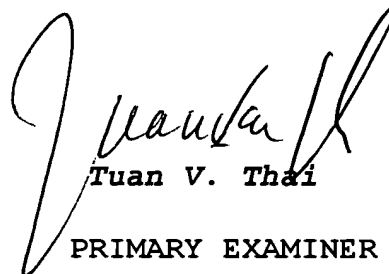
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be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/May 28, 2004



Tuan V. Thai

PRIMARY EXAMINER

Group 2100